MOLECULAR MEMORY INTEGRATED CIRCUIT UTILIZING NON-VIBRATING CANTILEVERS

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"Express Mail" mailing label number: EV327622965US
Date of Mailing: October 14, 2003

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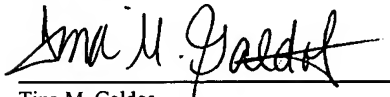

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Tina M. Galdos
Signature Date: October 14, 2003

Attorney Docket No.: LAZE-1011US1 SRM/MLR
Express Mail. No.: EV327622965US
MRobbins/LAZE/1011us1/1011us1.app.wpd

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PRIORITY CLAIM

[0002] This application claims priority to the following U.S. Provisional Patent Applications:

[0003] U.S. Provisional Patent Application No. 60/418,616 entitled "Molecular Memory Integrated Circuit Utilizing Non-Vibrating Cantilevers," Attorney Docket No. LAZE-01011US0, filed October 15, 2002.

[0004] U.S. Provisional Patent Application No. 60/418,618 entitled "Molecular Memory Integrated Circuit," Attorney Docket No. LAZE-01016US0, filed October 15, 2002.

CROSS-REFERENCE TO RELATED PATENT APPLICATIONS

[0005] This application incorporates by reference all of the following co-pending applications:

[0006] U.S. Patent Application No. _____, entitled "Atomic Probes and Media for high Density Data Storage," Attorney Docket No. LAZE-01014US1, filed herewith;.

[0007] U.S. Patent Application No. _____, entitled "Fault Tolerant Micro-Electro Mechanical Actuators," Attorney Docket No. LAZE-01015US1, filed herewith;

[0008] U.S. Patent Application No. _____, entitled "Phase Change Media for High Density Data Storage," Attorney Docket No. LAZE-01019US1, filed herewith;

[0009] U.S. Provisional Patent Application No. 60/418,923 entitled "Atomic Probes and Media for High Density Data Storage," Attorney Docket No. LAZE-01014US0, filed October 15, 2002;

[0010] U.S. Provisional Patent Application No. 60/418,612 entitled "Fault Tolerant Micro-Electro Mechanical Actuators," Attorney Docket No. LAZE-01015US0, filed October 15, 2002; and

[0011] U.S. Provisional Patent Application No. 60/418,619 entitled "Phase Change Media for High Density Data Storage," Attorney Docket No. LAZE-01019US0, filed October 15, 2002.

BACKGROUND OF THE INVENTION

Field of the Invention

[0012] This invention relates to memory on data storage devices and in particular in molecular memory integrated circuits. More particularly, the invention relates to molecular memory integrated circuits for use in micro-electro mechanical systems (MEMS).

Description of the Related Art

[0013] Current generation computer systems use separately manufactured integrated circuits and components assembled on or connected with system boards. Non-volatile data storage is one of the most performance critical components in a computer system. Current systems suffer from data storage technology incapable of matching the performance of other system components, such as volatile memory and microprocessors. Next generation systems will require improved performance from data storage devices.

[0014] Nearly every personal computer and server in use today contains one or more hard disk drives for permanently storing frequently accessed data. Every mainframe and supercomputer is connected to hundreds of hard disk drives. Consumer electronic goods ranging from camcorders to TiVo® use hard disk drives. While hard disk drives store large amounts of data, they consume a great deal of power, require long access times, and require "spin-up" time on power-up.

[0015] FLASH memory is a more readily accessible form of data storage and a solid-state solution to the lag time and high power consumption problems inherent in hard disk drives. Like hard disk drives, FLASH memory can store data non-volatilely, but the cost per megabyte is dramatically higher than the cost per megabyte of an equivalent amount of space on a hard disk drive, and is therefore sparingly used.

[0016] Current solutions for data storage cannot meet the demands of current technology, and are inadequate and impractical for use in next generation systems, such as MEMS. Consequently, it would be desirable to have an integrated circuit that stores data non-volatilely, that can be accessed instantaneously on power-up, that has relatively short access times for retrieving data, that consumes a fraction of the

power consumed by a hard disk drive, and that can be manufactured relatively cheaply. Such an integrated circuit would increase performance and eliminate wait time for power-up in current computer systems, increase the memory capacity of portable electronics without a proportional increase in cost and battery requirements, and enable memory storage for next generation systems such as MEMS.

SUMMARY OF THE INVENTION

[0017] A molecular memory integrated circuit includes a set of actuators capable of moving a platform. One embodiment in accordance with the present invention includes a plurality of actuators and platforms. The platform can contain either a memory device or a Molecular Array Read/Write Engine (MARE) with a cantilever system, which includes a cantilever tip. When a first platform with a memory device is brought within close proximity of a second platform with a MARE, the actuators can position the cantilever tip to a specific location on the memory device. The tip of the cantilever can perform a number of functions to the memory device, including reading the state of the memory device or changing the state of the memory device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] Further details of the present invention are explained with the help of the attached drawings in which:

[0019] FIG. 1 is a die of an embodiment of the invention that includes a number of cells where each cell further includes an interconnect, an actuator, a pull-rod, and a platform.

[0020] FIG. 2 is a cell of the embodiment of the invention of FIG. 1 that includes a MARE.

[0021] FIG. 3 is a scanning electron microscope picture of a cell of the embodiment of the invention of FIG. 1 including a MARE.

[0022] FIG. 4 is a cell of the embodiment of the invention that includes a memory devices.

[0023] FIG. 5a is a schematical representation of an embodiment of the invention with two platforms, one above the other, where the top platform holds a MARE with a cantilever system and the bottom platform holds a memory device.

[0024] FIG. 5b is the schematical representation of FIG. 5a with a tip of a cantilever on a platform holding a MARE making contact with a memory device that is held by a second platform.

[0025] FIG. 6 is a gross positioning grid of an embodiment of the invention.

DETAILED DESCRIPTION OF THE DRAWINGS

[0026] Referring to FIG. 1, die 100 is a device that includes sixteen cells 118 as well as many interconnect nodes 102 and many interconnects 104. Each cell 118 includes four actuators 106, four pull-rods 110, a platform 108, and sixteen cantilevers 112. The interconnect node 102 can be coupled with interconnect 104, which in turn is coupled with at least one of the cells 118. Interconnect 104 is also connected with various structures on the individual cells 118. For instance, an interconnect 104 is connected with the platform 108. Another interconnect 104 is connected with cantilever 112. Yet another interconnect is connected with actuator 106. Actuator 106, however, is also connected with pull-rod 110. Pull-rod 110 is also connected with platform 108.

[0027] Interconnect 104 can be made from any number of conductive materials. For instance, interconnect 104 could be made from aluminum or copper. Yet, as discussed below, the material chosen for interconnect 104 should have a higher coefficient of expansion than the material chosen for the arms of actuator 106.

[0028] Interconnect nodes 102 provide access to the die 100 from sources outside of the die 100, and interconnects 104 provide the pathway for outside sources to communicate with individual cells 118 and the components contained on such cells 118. For instance, sense and control signals can be passed to and read from actuator 106 to determine its relative position from a neutral state. Different signals can be sent to a cantilever 112 to determine the position of cantilever 112 and/or direct the cantilever 112 to read and/or write data to a memory device. Also, the position of platform 108 can also be detected by devices not included on die 100 through signals passed through interconnect node 102 and interconnect 104. Many other signals and readings can be made through interconnect node 102 and interconnect 104 as desired by the design of the die 100, the design of the system incorporating die 100, and other design goals.

[0029] In addition to sensing the location of platform 108 and actuators 106 through interconnect node 102 and interconnect 104 on die 100, control signals can be passed through interconnect node 102 and interconnect 104 to direct the actuators 106 to perform some action. For instance, a stimulus can be sent by an outside device directing a particular actuator 106 to actuate, moving only one platform 108 along either the X-axis or Y-axis as defined by reference 119. A control signal could also be directed to one or more actuators 106 at the same time directing multiple platforms 108 to move in different directions along

the X-axis, different directions along the Y-axis, in different directions in both the X-axis and Y-axis, or in the same direction as defined by reference 199. The sixteen cells 118 on die 100 can all be controlled simultaneously, individually, or they can be multiplexed. If cells 118 are multiplexed, then additional multiplexing circuitry is required.

[0030] Any of the structures can be multiplexed through the use of multiplex diodes, either on the device or external to the device. In addition, multiplexing can be accomplished through the use of transmission gates or other switching components such as simple MOSFETs.

[0031] The ability of the devices to operate multiple cells simultaneously and asynchronously is an advantage over previous art. Multiplexing is an advantage in server applications, for example, where multiple simultaneous accesses can be required at different memory locations within one block of memory. The smaller cell sizes, typically 32Mbytes versus a typical hard disk drive size of 20Gbytes and above, and the ability to access any of these small blocks simultaneously with any other, provide a typically 1000x granularity improvement over the use of hard disk drives in server applications. In addition, these devices exhibit access times typically 10x faster than hard disk drives. A typical access time is 500 μsec for these devices.

[0032] Another advantage of the multiple small storage cells or platforms is that the physical size of the media and head platforms is reduced greatly from larger platform implementations (such as described by IBM in their Millipede effort). The smaller platforms have much less thermal expansion than larger platforms. Also, thermal oxides or glass can be used for both the small media and head platforms further reducing thermal expansion or thermal mismatch problems, especially when compared with using silicon

as a platform substrate, which has about 10x the thermal expansion coefficient of glass. The multiple small platforms using glass type substrates allow the invention to operate over industrial temperature ranges without thermal compensation (heater or cooler). For example, where data is written to the media platforms in tracks, drift in alignment between the cantilevers 112 and tracks caused by thermal expansion can be a fraction of the track spacing of 20-25 nm (for example) across industrial temperature ranges. Because of low thermal expansion, cantilevers 112 can remain aligned with previously written tracks over a range of operating temperatures.

[0033] In addition the multiple cell access capability introduces performance advantages when used as cache memory in a computing environment. Cache memory can sit between the main memory and the collection of hard disk drives in a computing environment. Cache memory provides the ability to start frequently accessed information stored on the hard disk drives, with the ability to transfer information to main memory much faster than the hard disk drives themselves. The non-volatile nature of cache memory enables systems to power-down and power-up the computing environment much faster than systems using hard disk drives but not cache memory, and cache memory is much less expensive in cost per bit than FLASH memory. Use of cache memory has major advantages, particularly for portable applications where power savings are critical. Devices utilizing cache memory also inherently require less power than other devices, because the actuators require much less power than hard disk drives and can be powered up and down nearly instantaneously, with only the access time as the latency for powering up. Further, it is advantageous for cache memory to have a high data transfer rate to operate between the main memory (e.g. DRAM) and the hard disk drive. Multiple platforms operating in parallel can have an extremely high

data rate. For example, sixteen platforms operating in parallel can have greater than eighty megabytes per second read and write transfer rate.

[0034] As shown in FIG. 1, cells 118 do not require multiplexing and, therefore, do not contain any multiplexing circuitry.

[0035] In addition to cells 118, die 100 can also include any number of test structures. For instance, test circuitry 114 provides the ability to ensure that the manufacturing process for the actuator arms was performed correctly. A test signal can be applied to test circuitry 114 and a reading/measurement taken of the expansion rates of the arms of actuator 106, without potentially damaging any of interconnect nodes 102. Likewise, a test signal can be applied to test actuator 116 and a reading/measurement taken to determine the maximum force that test actuator 116 can apply to a pull-rod 110. Other data can be collected as well, such as the reliability of the manufacturing process, testing for potential reliability of die 100, determining the stress limits of test actuator 116 or the current requirements in order to induce test actuator 116 to move. Any number of different tests can be designed for test circuitry 114 and test actuator 116 beyond those identified here. Also, other test structures besides test circuitry 114 and test actuators 116 can be included on die 100.

[0036] While die 100 includes an array of four by four (4x4) cells 118, many other alternate designs could also be fabricated for die 100. For instance, a single row of sixteen cells 118 could be manufactured and identified as die 100. Also, die 100 could contain as few as a single cell 118 or as many cell 118 as the manufacturing process permits on a single wafer. As semi-conductor manufacturing processes change so that greater die densities and larger wafers can be made, a greater number of cells 118 can be included on a single die 100.

[0037] Additionally, while cells 118 in die 100 include platforms 108 with cantilevers 112, cells 118 in die 100 could also be made that have platforms 108 that include memory devices. Furthermore, die 100 could include a first group of cells 118 with platforms 108 that include cantilevers 112 and a second group of cells 118 with platforms 108 that include memory devices.

[0038] FIG. 2 is a cell 218, which is an extract from cell 118 from FIG 1 where cell 118 includes a Molecular Array Read/Write Engine (MARE). X-left actuator 222 is coupled with pull-rod left 220, which is in turn coupled with platform 208. Y-top actuator 226 is coupled with pull-rod top 224, which is in turn coupled with platform 208. X-right actuator 228 is coupled with pull-rod right 230, which is in turn coupled with platform 208. Y-bottom actuator 232 is coupled with pull-rod bottom 234, which is in turn coupled with platform 208. Interconnect 204 is coupled with platform 208. While not shown in complete detail, but following FIG. 1, interconnect 204 is also coupled with X-left actuator 222, Y-top actuator 226, X-right actuator 228 and Y-bottom actuator 232. Furthermore, platform 208 is coupled with cantilever 212. As can be seen in FIG. 2, this particular figure displays sixteen cantilevers 212. Moreover, interconnect 204 is includes one or more interconnections that taken in combination are identified as interconnect 204.

[0039] Cantilevers 212 can be designed several different ways. One method is to manufacture the cantilevers 212 such that they have their own, independent directional control system. Thus, cantilevers 212 could be designed to be capable of moving along all three axises as defined by reference 299 (x-axis, y-axis, and z-axis). Such a design would require additional interconnections 204 in order to allow control signals to direct cantilevers 212.

[0040] Yet another cantilever 212 design is to make the cantilever 212 such that it does not require any independent stimulation to maintain contact with a desired target, or a passive cantilever 212.

For instance, the cantilevers 212 are included in a MARE (Molecular Array Read/Write Engine), which is in turn connected with a platform 208 that is part of a cell. The cell can be moved along the Z-axis, as defined by reference 299, such that the cantilever 212 makes contact with a target platform. Cantilever 212 is then designed to have a curvature such that it curves away from the plane defined by platform 208. Thus, when looking at platform 208 from the side, cantilever 212 will protrude away from platform 208. Consequentially, as a target platform is positioned in close proximity to platform 208 and cantilever 212, the tip of cantilever 212 will make first contact with the target platform. Cantilever 212 can be designed such that it has a spring like response when pressure is placed upon the cantilever 212 tip. Hence, small changes in the distance between platform 208 and the target platform will not cause cantilever 212 from breaking contact with the target platform. The tip of cantilever 212 can then be positioned within the X/Y plane, as identified by reference 299 and defined by the target platform, through movement of platform 208 by the actuators (X-left actuator 222, Y-top actuator 226, X-right actuator 228, and Y-bottom actuator 232). Additionally, the relative X/Y location of the tip of cantilever 212 to the target platform can also be changed by movement of the target platform in the X/Y plane as defined by the target platform and as referenced by reference 299.

[0041] Another option is to make platform 208 so that it is spring loaded. Thus, cantilever 212, which is coupled with platform 208, contacts the target platform, both platform 208 and the target platform could move in the Z-direction. In this mode, fine probe tips (cantilever tips) are formed on cantilever 212 and arrayed around platform 208 to distribute the loading forces of platform 208 on the target platform. This reduces the amount of wear on both the fine probe tips and the target platform.

[0042] Yet another option is to place platform 208 inside a recessed cavity. This will provide additional space to permit the platform 208 to move in the Z-direction either through stimuli from the actuators or any spring loading incorporated into platform 208.

[0043] FIG. 3 is a scanning electron microscope picture of a cell 118 from FIG. 1. X-left actuator 322 is coupled with pull-rod left 320, which is in turn coupled with platform 308. Y-top actuator 326 is coupled with pull-rod top 324, which is in turn coupled with platform 308. X-right actuator 328 is coupled with pull-rod right 330, which is in turn coupled with platform 308. Y-bottom actuator 332 is coupled with pull-rod bottom 334, which is in turn coupled with platform 308. Interconnect 304 is coupled with platform 308. While not shown in complete detail, but following FIG. 1, interconnect 304 is also coupled with X-left actuator 322, Y-top actuator 326, X-right actuator 328 and Y-bottom actuator 332. Moreover, interconnect 304 is includes one or more interconnections that taken in combination are identified as interconnect 304. Also shown in FIG 3. Is a MARE (Molecular Array Read/Write Engine) with sixteen cantilevers 340 each with a cantilever tip 342.

[0044] FIG. 3 shows how cantilever 340, which is coupled with platform 308, extends away from platform 308 in the Z-direction as defined by reference 399. At the end of cantilever 340 is a cantilever tip 342. Cantilever tip 342 is the point of contact with a target platform that is brought into close proximity with platform 308. For instance, if a memory device on a target platform is brought into close proximity to platform 308, eventually cantilever tip 342 will make contact with the memory device. For the cell shown in FIG. 3, since there are sixteen cantilevers 340, each with its own cantilever tip 342, there will be sixteen points of contact when the target platform is brought into contact with platform 308. Each cantilever

340 can handle a load force within reasonable limits. For instance, when a target platform makes contact with a cantilever tip 342, the cantilever 340 holds a contact load exerted by the target platform. As a consequence, cantilever 340 is designed to handle some deflection from its position with no load applied. Cantilever 340 is spring loaded such that as a force is applied to the cantilever tip 342, cantilever 340 applies a force back at the target platform, which is asserting the force which has caused cantilever 340 to move from its original position. Consequentially, small movements along the Z-axis as defined by reference 399 will not cause the cantilever tip 342 to break contact with the target platform. Only when the target platform asserts no force against cantilever tip 342 can contact break between cantilever tip 342 and the target platform.

[0045] This design provides error control and durability to the design. Such a design could be adjusted to handle a wide range of error forces that could break contact between cantilever tip 342 and the target platform. The hardness of the cantilever tip, the hardness of the device on the target platform, and the friction coefficients of the two materials are several factors determining how much force the cantilever tip 342 can be subject to before the overall functionality of the micro-electronic mechanical system (MEMS) is impaired. For instance, in a MEMS device designed as a memory device such that the target platform holds a memory device that can be read and written to by the cantilever 340 through the cantilever tip 342, the cantilever tip 342 should be designed to minimize scratches, scars, deformities, etc., caused by cantilever tip 342 to the memory device. Likewise, the cantilever tip 342 must not be to soft as to be damaged by the memory device on the target platform.

[0046] FIG. 4 is a cell 418 that includes memory devices as opposed a MARE (Molecular Array Read/Write Engine) with cantilevers. X-left actuator 422 is coupled with pull-rod left 420, which is in turn coupled with platform 408. Y-top actuator 426 is coupled with pull-rod top 424, which is in turn coupled with platform 408. X-right actuator 428 is coupled with pull-rod right 430, which is in turn coupled with platform 408. Y-bottom actuator 432 is coupled with pull-rod bottom 434, which is in turn coupled with platform 408. Interconnect 404 is coupled with platform 408. While not shown in complete detail, but following FIG. 1, interconnect 404 is also coupled with X-left actuator 422, Y-top actuator 426, X-right actuator 428 and Y-bottom actuator 432. Moreover, interconnect 404 includes one or more interconnections that taken in combination are identified as interconnect 404. Additionally, memory devices 450 is coupled with platform 408. Shown in FIG. 4 are sixteen memory devices 450.

[0047] The actuators (X-left actuator 422, Y-top actuator 426, X-right actuator 428 and Y-bottom actuator 432) behave as described for the actuators of FIG. 2. Thus, as the actuators (X-left actuator 422, Y-top actuator 426, X-right actuator 428 and Y-bottom actuator 432) are activated, they exert a force along their corresponding pull-rod (pull-rod left 420, pull-rod top 424, pull-rod right 430, pull-rod bottom 434), respectively. Thus, platform 408 can be moved within the X-Y plane defined by platform 408 and referenced by reference 499. Furthermore, all of the actuators (X-left actuator 422, Y-top actuator 426, X-right actuator 428, and Y-bottom actuator 432) include the fault tolerant design discussed in FIG. 2.

[0048] FIG. 5a is a side view of a portion of a platform 508 holding a MARE (Molecular Array Read/Write Engine) 556 from a cell like cell 218 depicted in FIG. 2 positioned over a platform 554 from

a cell like cell 418 depicted in FIG. 4 with a memory device 558. As can be seen, cantilever 540 has a curve, which causes cantilever 540 to extend along the Z-axis, as defined by reference 599. The furthest point from platform 508, but still coupled with platform 508, is cantilever tip 542. Cantilever tip 542 is the point that will contact the target device, in this case memory device 558, which is coupled with platform 554.

[0049] In operation, as shown in FIG. 5b, platform 508 and platform 554 are brought together such that the cantilever tip 542 of cantilever 540 comes in contact with memory device 558. In a typical memory access, a relatively large movement takes place such that the cantilever tip 542 is placed in one of nine quadrants relative to the memory device 558. For instance, in FIG. 6 is shown a top view of a memory device 619 which corresponds to memory device 558 in FIG. 5a and 5b. The memory device 619 is sectioned into nine sections: top left 601, top middle 603, top right 605, center left 607, center middle 609, center left 611, bottom left 613, bottom middle 615, and bottom right 617. Thus, for a memory access, cantilever tip 542 is first moved to one of the quadrants. For example, for a memory read someplace within the top right quadrant 601, cantilever tip 542 is positioned into the top right quadrant 601. This positioning can be performed in a number of different ways. For instance, platform 508 can be moved by way of actuators like those in FIG. 2. When platform 508 is moved, then the cantilever 540 that is coupled with platform 508, consequently, moves as well. Eventually, cantilever 540 will be positioned such that cantilever tip 542 will be within the top right quadrant 601. After gross positioning of cantilever tip 542, then fine positioning commences so an individual data bit can be read or written to by cantilever 540 through cantilever tip 542.

[0050] Another method is to move platform 554 by activation of actuators, such as those in FIG. 4, so that the memory device 558 is moved so as to bring the top right quadrant 601 to a position where cantilever tip 542 makes contact with the memory device 558 inside of top right quadrant 601. Yet another method is to move both platform 508 and platform 554 to bring cantilever tip 542 into the top right quadrant 601 of FIG. 6. Similar methods can be used for the remaining quadrants. Also, the memory device 558 could be broken into different formations. For instance, memory device 558 could be broken into three rectangular regions, three horizontal regions, one horizontal region and three smaller vertical regions for four total regions, etc. Again, after a gross positioning step, then fine movements are made to isolate a single data bit. Yet another method would be to skip the gross positioning step and rather make fine, precise movements to a particular location. Gross positioning and fine positioning can also proceed concurrently.

[0051] The foregoing description of the present invention have been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Obviously, many modifications and variations will be apparent to practitioners skilled in this art. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, thereby enabling others skilled in the art to understand the invention for various embodiments and with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the following claims and their equivalents.